## REMARKS

Claims 1, 3 and 8 are active. Claims 2, and 4-7 are canceled. Claim 1is rejected under 35 USC 102 as being anticipated by Kawamoto '098. Claims 1-4 and 8 (claims 2 and 4-7 being canceled) are rejected under 35 USC 102 as being anticipated by Nomura '068. Claims 5 and 6 (canceled) are rejected under 35 USC 102 as being unpatentable over Nomura in view of Bortscheller '001. Claim 7 (canceled) is rejected under 35 USC 103 as being unpatentable over Nomura in view of Ker '1146.

Amended claims 1, 3 and 8 are submitted for the examiner's reconsideration.

Claim 1 is amended to include certain of the subject matter of canceled claims 2 and 5, which are canceled for this reason. Claims 4 and 7 are inconsistent with the amended claim 1 and are canceled for this reason, that is claim 1 calls for capacitive coupling of the gate electrode of the charging transistor to one of the source/drain electrodes. Claims 4 and 7 call for resistive coupling, which is different than the capacitive coupling of amended claim 1 and thus are canceled. Claim 6 is redundant with claim 3 in view of the amendment to claim 1 and is canceled for this reason.

Amended claim 1 is not suggested, disclosed or otherwise made obvious by any of the cited references of record including '098, '068, '001 or '1146 taken individually or in combination. Amended claim 1 calls for:

> at least one organic charging field effect transistor (charging FET) on a substrate, . . . and at least one switching organic field effect transistor (switching FET) . . . such that the gate electrode of the charging FET is not connected via an electrical line directly to the voltage source, to the reference potential, to the input or to the output, wherein the gate electrode of the charging FET is directly capacitively coupled to one of the source/drain electrodes of the charging FET (underlining added)

'098 does not disclose an organic FET, but an inorganic device. The substrate is silicon, col. 2, line 1 and the gate insulating film is $SiO_2$, inorganic materials. As stated in applicants' specification at page 1, lines 6-8, " The present invention relates to the problem of the switching times and the switching stability of organic logic gates, and at lines 30-32, "No organic logic gate circuits have been realized hitherto which can switch rapidly and stably even with low supply voltages." And at lines 34 et seq. page 1, applicants' specification states "For reasons of energy efficiency it is desirable to lower the supply voltages of organic logic gate circuits even during fast operation of organic circuits, without impairing the switching stability in the process." Therefore '098 does not recognize the problem with organic devices in such a circuit as claimed and thus is of no help in the solution.

Also, claim 1 calls for the gate electrode of the charging FET to be directly capacitively coupled to one of the source/drain electrodes of the charging FET. This structure is missing in '098, as there is no capacitive coupling disclosed in this reference as claimed. Thus claim 1 amended is believed allowable over this reference.

'068 is also foreign to amended claim 1. This reference also shows an inorganic device and thus this reference also does not recognize the problem nor the claimed solution of amended claim 1. The disclosed device is a CMOS device. This is a metal oxide semiconductor device, which is inorganic. Thus claim 1 is allowable at least for this reason alone.

However, claim 1 calls for more. Claim 1calls for "the gate electrode of the charging FET is not connected via an electrical line directly . . . to the input" and the gate is also "directly capacitively coupled to one of the source/drain electrodes of the

charging FET." Neither of these structures are disclosed or suggested by '68. The gate electrodes of both the p1 and n1 devices are connected to each other and to a common input and the gate electrodes are not directly capacitively coupled to either a source or drain electrode, but rather via a series connected resistance. This is different. Thus claim 1 is believed allowable over this reference for this reason.

As to the cited '001 reference, this does not show a series connection of a charging transistor and a switching transistor as claimed, but is merely cited to show overlap of the gate electrode with the source/drain electrodes. Also, such overlap is contradictory to the reason for applicants' claimed overlapping. The '001 reference states at col. 3, lines 51-52, "The FIG. 3 electrode arrangement also provides low source-to-gate and drain-to-gate capacitance values." (underlining added) These values are "less than 10-13 Farads", col. 3, line 58, and thus therefore "unwanted signal coupling between source 318 and drain 328 electrodes is reduced." This is not what is claimed and teaches away from amended claim 1. This '001 coupling is reduced because this reference teaches minimum 3 micron widths 322 and 324 (Fig. 3) of the source and drain electrodes with the gate electrode 314. This structure is contrary to applicants claimed capacitive coupling.

For example, in applicants' figure 4 the gate electrode is gate 20 and one of the drain/source electrodes is electrode 8. Applicants' specification states at page 6, lines 29 et seq. that "the region 16 essentially defines the region of the capacitive coupling between the gate electrode 20 and the electrode 8." This is larger than and thus is

totally different than the minimum 3 micron widths of the drain/source electrodes of the '001 reference between the minimized coupling between the source/drain electrodes and the gate. Such a minimized capacitive coupling (referred to as parasitic capacitance in the reference ) is not the same as or as desired in applicants' claim 1 structure. Also, the transistor of the '001 reference is not disclosed or suggested for use in a switching device as claimed in amended claim 1 and teaches away from such structure for the reason given. Teaching away is the antithesis of obviousness. Amended claim 1 is believed allowable over this reference for these reasons.

Ker '1146 is cited for the resistive coupling of the canceled claims 4 and 7. This structure is not included in amended claim 1. Therefore, this reference is moot as to amended claim 1. Applicants have carefully reviewed this reference and also fail to find any relevance to amended claim 1. If the examiner persists in citing this reference, he is respectfully requested to point out with particularity its relevance to amended claim 1. None of the cited references taken individually or in combination thus teach or suggest amended claim 1. This claim is believed allowable.

Claims 3 and 8 depend from claim 1 and are believed allowable for at least this reason. Claim 3 is directed to the overlapping of the gate electrode with one of the drain and source electrodes. This is believed additionally novel over the cited references of record and especially the '001 reference for the reasons discussed above.

Since claims 1, 3 and 8 have been shown to be in proper form for allowance, such action is respectfully requested.

No fee is believed due for this paper. However, the Commissioner is authorized to respectively charge or credit deposit account 03 0678 for any under or overpayments in connection with this paper.

Respectfully submitted,
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